使用DDR SDRAM，你的阻抗范围有多大？阻抗值的范围，即接口可正常运行的电路板容限，通常是不确定的。因此，制造商使用尽可能大的电路板容限，以尽可能降低制造成本。新的试验显示，可在比现有设计惯例建议的阻抗更大的范围内使用DDR SDRAM。对完全匹配的传输线，唯一的限制看来是信号长度应远远长于一英寸。

DDR SDRAM CHARACTERISTIC IMPEDANCE and PCB Design

How much impedance variation can a DDR SDRAM interface tolerate before going out of spec? by CHARLES GRASSO and FRANCES WU

As clock speeds increase and rise times decrease, the importance of maintaining good signal integrity in electronic products has assumed increasing importance and visibility. This is particularly true of the ubiquitous products incorporating DDR SDRAM devices.

The characteristic impedance of the circuit board under design is usually the first, and arguably the most important, design parameter. The question remains, however: How does a design engineer determine the optimal characteristic impedance for a DDR SDRAM design? Typically, the design engineer will refer to design guides published by either the DDR SDRAM manufacturer or the memory controller manufacturer for implementation recommendations, or simply copy a reference design. However, technical notes can be singularly unhelpful when faced with actually engineering a product and simply copying a reference design will not ensure a manufacturable solution.

To underline the impedance selection difficulties, some technical notes with layout recommendations for DDR SDRAM typically recommend that the characteristic impedance of the interface should be 50 Ω[2], while others don't give any recommendations whatsoever[3], leaving design engineers to use their best judgment.

As an added complication, the range of impedance values, i.e., the board tolerance with which the interface can be considered to work properly, is typically not defined. As a consequence, the widest possible board tolerances are used in order to keep manufacturing costs as low as possible. Typical desired board impedance tolerances are in the ±10% range – with pressure for larger variances from the manufacturers to keep costs down. Variances in characteristic impedance result in undesired reflections, for example a ±10% change in char-

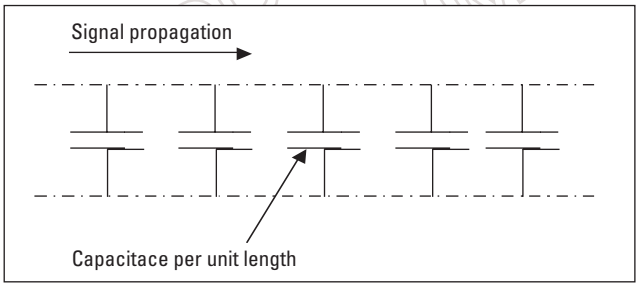

FIGURE 1. Capacitor model of a transmission line.

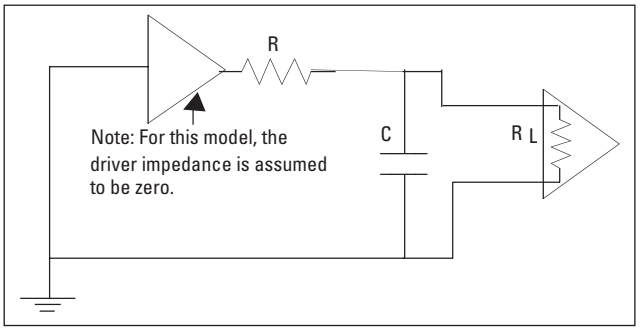

FIGURE 2. A transmission line described in terms of capacitance.

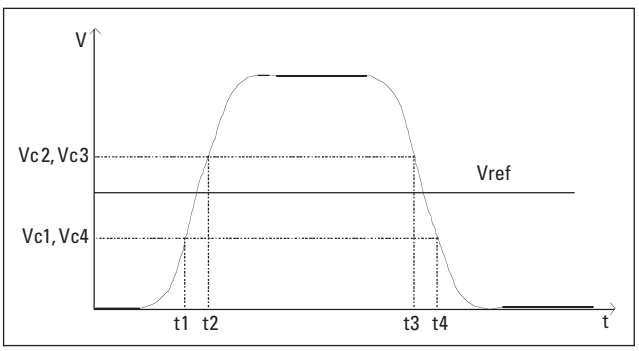

FIGURE 3. Calculating the slew rate using RC response formula.

TABLE 1. Calculated capacitance of transmission line with different characteristic impedance

ZO (Ω)	CO (pF/in)
10	14.02
20	7.023
30	4.682
40	3.512
50	2.81
60	2.34
70	2.01
80	1.76
90	1.56

acteristic impedance will result in a ±5% signal reflection[5]. Recent publications recommend characteristic impedance variations of no greater than ±5% to assure low noise margins[4].

In order to ascertain how much impedance variation a DDR SDRAM interface can tolerate before going out of specification, and hence how much freedom a designer has when laying out the interface, a study of a 133 MHz DDR SDRAM for slew rate and crosstalk was completed using traditional circuit analysis and simulation.

Slew rate is the edge rate (rate of change of a signal voltage with respect to time) measured between two defined voltage levels. For DDR SDRAM, the slew rate is measured from the V_{IL} (input low voltage) to V_{IH} (input high voltage) on the rising and falling edges. For example, Micron specifies the slew rate of a 256 MB device as a minimum of 0.5V/ns for command and address lines. If the slew rate is exceeded, then the timing parameters are adjusted to ensure a valid data window. If the slew rate exceeds 4.5V/ns, the system functionality is uncertain[8]. The characteristic impedance of a PCB should directly affect the slew rate (or rise/fall time) of a signal, with the capacitance of signal path being the most dominant factor.

First evaluated was the effect of the characteristic impedance changes using the basic capacitance charge and discharge equations. Then data trends were plotted. This was then followed by a more extensive and exact analysis using an Ansoft SpiceLink 2D finite element solver with the BGA IBIS model, and then the results were compared.

Analysis of a Lumped Capacitor Model

Any two conductors form a transmission line, whose properties are determined by the geometry of the conductor pair and the medium in which the signal propagates. Characteristic impedance is a parameter of every uniform transmission line that is proportional to the voltage applied, and the current required to charge the line – which in turn is proportional to the capacitance of the line[7]. Typically, transmission line parameters are described in units/length. Therefore we can visualize the charging effect by building a simple model of a transmission line as an array of capacitors shown in **FIGURE 1**.

As the signal propagates along the transmission line, the rise time of the signal will be degraded by each unit capacitance. Discounting transmission line effects such as reflections, it is reasonable to assume (at least for a first-order approximation) that the rise time of a signal at the end of the transmission line can be estimated using the total capacitance of the line.

Line drivers are typically specified with a total load capacitance (of which the transmission line is one component) to meet the specified rise and fall time. Using a lumped approximation and ignoring transmission line effects, we should be able to get a good first-order model to estimate the effect of transmission lines of various lengths on the signal rise and fall times.

The microstrip transmission line is a simple geometric structure consisting of a trace over a ground plane with the characteristic impedance generally given by

$$Zo = \sqrt{\frac{R + jwL}{G + jwC}} \qquad \text{Eq. 1}$$

Where
R= series resistance of line, Ω/in
L = series loop inductance of line H/in
G = parallel conductance of line, mhos/in
C = parallel capacitance of line F/in

Assuming a lossless transmission line, the characteristic impedance, Zo, simplifies to the following formula:

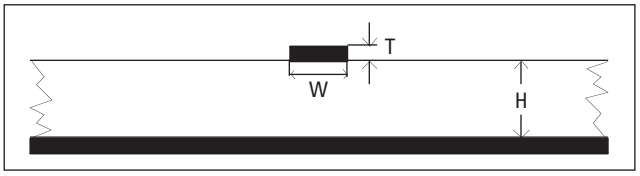

FIGURE 4. Microstrip parameters used to calculate capacitance.

$$Zo = \sqrt{L/C} \qquad \text{Eq. 2}$$

Referring to equation Eq. 2, it is clear that as the capacitance increases, Zo falls inversely and as the capacitance decreases Zo increases.

Connecting a driver to a transmission line with an appropriate series terminator forms a simple RC circuit as shown in **FIGURE 2**. In this case, the transmission line is represented by the capacitance, C, and the resistor, R, represents the series impedance. This simplified analysis cannot account for the effect of the transmission line loop inductance, which will cause the Zo to decrease as the loop inductance decreases with smaller loop area, and vice versa. Also, this analysis cannot account for any overshoot or undershoot that will result from large mismatches in the series termination and the transmission line.

As the input impedance, RL, of an integrated circuit is typically a high impedance, it is assumed that RL = ∞ and this analysis will not consider any effect due to RL. The rise time and fall time, or the slew rate, of a signal can now be found using the standard equations for charging and discharging a capacitor. For this analysis, the impedance of the output driver is assumed to be zero.

Charging:

$t_1 = -RC * \ln(1-Vc_1/Vs)$ Eq. 3

$t_2 = -RC * \ln(1-Vc_2/Vs)$ Eq. 4

$\Delta t = t_2 - t_1$ = Rise time Eq. 5

Discharging:

$t_3 = -RC * \ln(Vc_3/Vs)$ Eq. 6

$t_4 = -RC * \ln(Vc_4/Vs)$ Eq. 7

$\Delta t = t_4 - t_3$ = Fall time Eq. 8

Where $V_{c1} = V_{IL}$(max) on the rising edge
$V_{c2} = V_{IH}$(min) on the rising edge
$V_{c3} = V_{IL}$(max) on the falling edge
$V_{c4} = V_{IH}$(min) on the falling edge
Vs = Source voltage

The following equation can be used to calculate the capacitance of a microstrip for different characteristic impedances using the construction shown in **FIGURE 4**.

$$Co(pF/in) = \frac{0.67(Er + 1.41)}{\ln\left(\frac{5.98\ H}{0.8W + T}\right)} \qquad \text{Eq. 9}$$

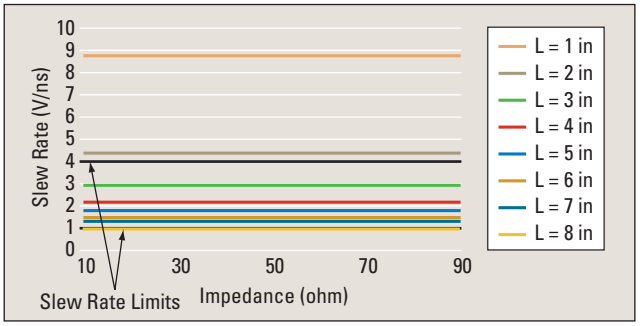

FIGURE 5. Effect of Zo and trace length on slew rate.

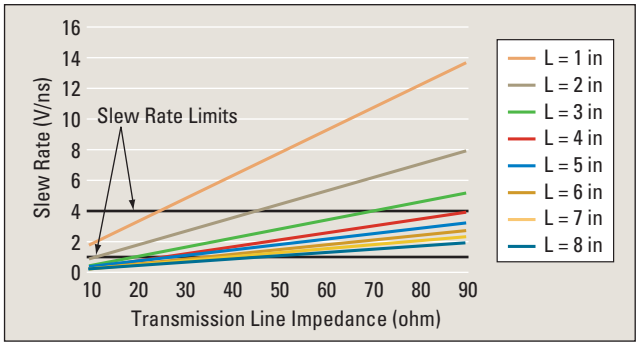

FIGURE 6. Signal slew rate with fixed series termination and different trace impedances.

Where Er = dielectric relative permittivity
H = trace height above ground
W = trace width
T = trace thickness

For example, on a standard multilayer PCB with a thickness, T, of .0014″ for 1 oz. copper and dielectric thickness, H, of .005″ and a trace width of .008″ the characteristic impedance is 50 Ω. The capacitance of this trace configuration can be calculated using Eq. 9 as 2.81pF/in. **TABLE 1** lists the calculated capacitance of the microstrip example with the different characteristic impedances obtained by varying H.

Once the value of capacitance per inch is found, calculating the capacitance of traces of various lengths is a simple matter of adding multiples of the unit measurement.

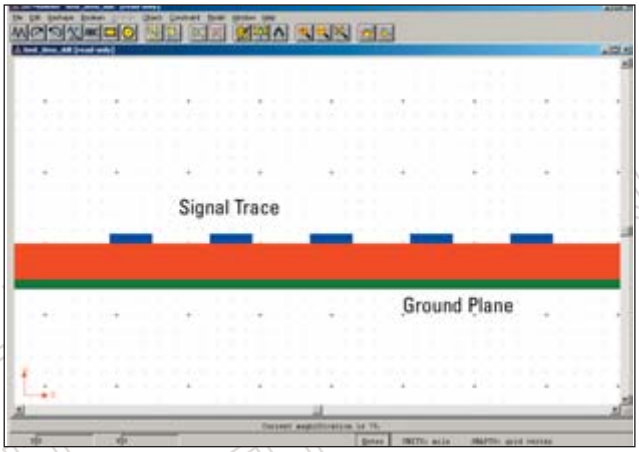

FIGURE 7. Transmission line cross-section shown with Ansoft SI2D extractor.

Ideal Case: Matched Source and Trace Impedance

Assuming the transmission line is terminated properly, the R in the RC-response formulae (Eq. 3, Eq. 4, Eq. 6 and Eq. 7), is set to match the characteristic impedance of the line. The capacitance, C, of the total transmission line length is calculated using the per unit length values from Table 1. A comparison of the slew rates calculated (Eq. 5 and Eq. 8) for transmission lines with different characteristic impedances is graphically depicted in **FIGURE 5**.

From the data sheets for a typical 133 MHz DDR SDRAM, the non-dated slew rate limits are specified as 1V/nS and 4V/nS[8]. The slew rate limits are depicted in Figure 5 as solid black lines. Some initial conclusions from this simple analysis can be made. First, trace lengths of one inch or less are not acceptable, as the slew rate will exceed the upper limit. Second, and somewhat surprisingly, the slew rate is significantly affected by varying the characteristic impedance thereby verifying that DDR SDAM can be used in widely varying board technologies as stated in the scope of the SSTL2 standard[1]. As a general rule – for properly matched transmissions lines (i.e., the ideal case) SDRAM DDR can be used with typical industry standard board impedances between 50 Ω and 100 Ω for trace lengths greater than 1 inch.

Non-Ideal Case: Mismatched Source and Trace Impedance

Because the characteristic impedance of the transmission line will vary over a manufacturing cycle, although the termination resistor has been pre-determined, the slew rate calculations (Eq. 5 and Eq. 8) were repeated with the R of the equation fixed (i.e., a fixed series impedance) and the C varied within a certain range (i.e., a variation in PCB stackup).

With the fixed series termination of 50 Ω (which implies a desired characteristic impedance set to 50 Ω), the transmission line impedance was varied and the results plotted in **FIGURE 6**. The data indicates that a PCB targeted for 50 Ω will not violate the slew rate requirements (for trace lengths about 2 inches long) with an impedance tolerance of ± 20%.

Referring to Figures 5 and 6, the results indicate that DDR SDRAM can be used over a wide range of board impedances. For perfectly matched transmission lines, the only limitation seems to be that the length of the signal should be much longer than 1 inch. Other than that, it appears that DDR

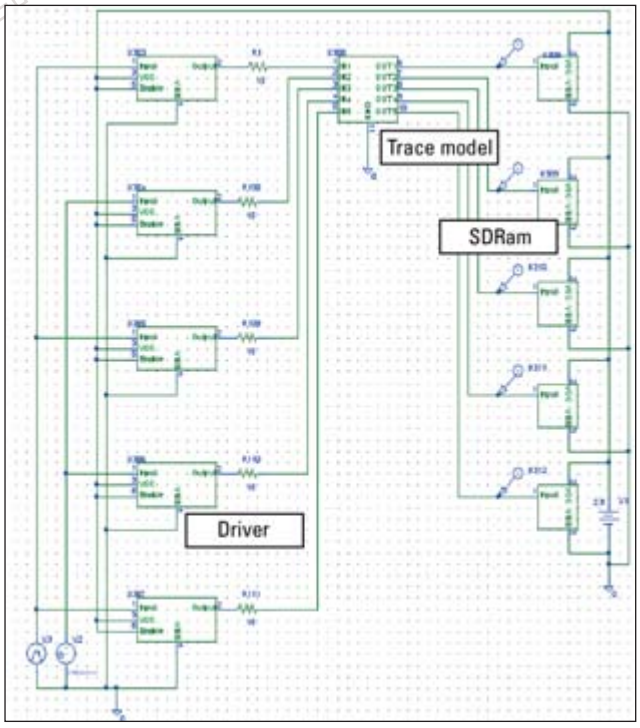

FIGURE 8. PSpice simulation setup.

SDRAM is tolerant of the actual characteristic impedance value. Furthermore, the calculations also indicate that DDR SDRAM is very tolerant of mismatched lines (not including the effects of ringing), implying that wide variations in the PCB and hence a cheaper design can be possible.

Simulating Slew Rate and Crosstalk

The set of lumped capacitor model calculations relied on the capacitive nature of the transmission line to calculate the signal slew rate. The calculations did not account for the effect of an actual driver, nor could it account for any mismatch, crosstalk or inductance effects that are dependant upon rise time and impedance.

For a more accurate representation, simulations on signal slew rate as well as crosstalk were performed to substantiate the calculated results using the IBIS model of a typical DDR SDRAM device driver and a behavioral model of the transmission line. The IBIS model of the device driver also includes inductive and resistive effects of the I/O pins and reflects the actual signal characteristics. The transmission line behavioral model recreates the electromagnetic environment of the transmission.

The DDR interface has two drive strengths from which a user chooses from: high (Class II) and weak (Class I). The output impedance of the driver changes depending on the drive strength – higher impedance for Class I (typically 35 Ω) and lower impedance for Class II (typically 17 Ω). All simulations were performed with both drive strengths.

In order to get the electromagnetic behavioral model of the transmission line, a configuration of five traces has been simulated using the Ansoft SpiceLink 2D finite element parameter extractor, as shown in **FIGURE 7**. The trace width was set to .006″ with a separation between the traces of .008″. By varying the dielectric thickness, the transmission line impedance can be varied in the range of 10 Ω to 90 Ω. The models were then imported into PSpice for simulation using the circuit configuration shown in **FIGURE 8**. Both the driver and receiver models were created using the IBIS model from the IC manufacturer to account for driver impedance in all simulations.

Simulations were performed first on the ideal case, (where the driver and series termination is set appropriately to match the transmission line impedance), as well the as non-ideal case, where series termination is set to a fixed value (33 Ω) and the trace impedance varied. The effect of crosstalk was also simulated using the excitation waveform depicted in **FIGURE 9**. Using this waveform captures all the crosstalk when the transitions are moving in phase, out of phase and when some lines are static.

The results of the simulations are graphically represented in **FIGURE 10**. The green blocks (light gray) represent configurations that comply with the DDR SDRAM slew rate specification and the red blocks (dark gray) mean the configuration fails the specification. Although not explicit, the degree of overshoot and undershoot can be extrapolated from the amount of crosstalk on adjacent lines. The data indicates that, typically, a design using the Class I driver is very tolerant of impedance variations and mismatches correlating with the observations of calculated results very nicely.

However, the data of a design using the Class II (lower impedance, higher drive strength) drivers are not so forgiving. The data indicates that if a design using Class II drivers is mismatched or uses a low impedance board design (e.g., 50 Ω), it will violate the DDR SDRAM slew rate specifications and suffer from crosstalk and ringing. Indeed, the Class II driver set only becomes usable as the board impedance increases.

At first glance this result seems counterintuitive but an examination of the transmission line analysis and model suggests an answer. The Ansoft 2D extractor finite element analysis tool features a current distribution feature known as adaptive meshing, which models the consequence to the loop inductance of proximity effect and skin effect as the separation between the trace and the ground plane is varied.

The total loop inductance of a transmission line can be represented by:

$$Lt = L_{trace} + L_{returnpath} - 2L_{mutual} \qquad \text{Eq. 10}$$

Where Lt = Total loop inductance
L_{trace} = Trace Inductance
$L_{returnpath}$ = Return path Inductance
L_{mutual} = Mutual Inductance

Therefore, as the mutual inductance gets larger (that is, as the trace gets closer to the plane and the characteristic impedances decrease), the overall loop inductance is reduced and the signal rise times get faster. As the mutual inductance gets smaller (that is, as the trace gets further from the plane and the characteristic impedances increases), the overall loop inductance increases and the signal rise times get slower.

The simulations also indicate that for low-impedance boards, other PCB design techniques that mitigate the slew rate requirements and crosstalk issues such as guard bands or trace separation will need to be employed. Adding sufficient series resistance to round off the signal can sometimes help, but this technique requires extensive measurement and experimentation.

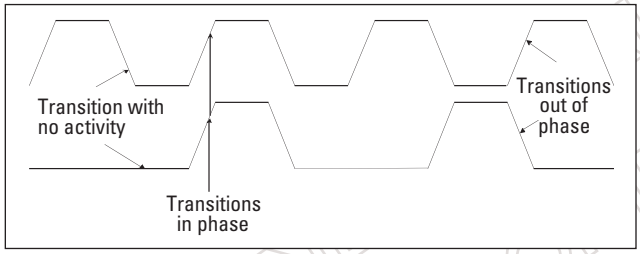

FIGURE 9. Excitation waveform for crosstalk analysis.

The impedance requirements of DDR SDRAM are tolerant to both the PCB characteristic impedance value and variations at least for Class I drive strengths. The situation is different for the Class II drive strengths, however, and the data indicates that mismatches in board impedance are not tolerated as well. Indeed, when the signal lines are properly terminated, the simulation indicates that a Class II design will fail the slew rate requirements on typical trace lengths. **PCD&M**

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FIGURE 10. Characteristic impedance variation and crosstalk simulation results.